IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 1, Issue 1, March, 2013
ISSN: 2320 - 8791
www.ijreat.org

Retiming Of Circuits Using Clock Management Techniques

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Abstract

Retiming is one of the most powerful sequential transformations that relocates flip-flops in a circuit without changing its functionality and that optimizes the sequential circuit which improves performance. It is the concept of improving the timing behavior of a circuit by relocating flip-flops across logic gates to achieve faster clocking speed. It decreases the iteration period without affecting functionality. A lower iteration period implies faster execution. This paper proposes different clock management techniques which were implemented in asynchronous counter to minimize the clock period. In this work net skew and maximum delay of the clock and average connection delay, maximum pin delay and connection delay on critical nets will be compared. The Xilinx ISE Design suite, Modelsim-Altera has been used for simulation and programming was done in VERILOG model.

Keywords--- *clock, retiming, iteration period, speed*

1.Introduction

Retiming is a sequential optimization technique that relocates flip-flops within a circuit without altering the functionality [1]. As relocating the flip-flops balances the critical path and reduces the states of the circuit, retiming transformation can be implemented to minimize the clock period. In this paper minimum clock period with retiming has been discussed. Clock signal, is playing important role in sequential circuits which is used for synchronization of data to the circuit [2]. The circuits using clock signal will become active at rising and falling edges of signal [3]. It has high frequency. Retiming to achieve minimum clock period is minimum period retiming. It has many applications in sequential circuit design which includes reducing clock period, reducing power consumption and logic synthesis. It can be used to increase the clock rate by reducing delay on critical path [4],[10]. However, interconnect delay and clock skew are the important factors to decide the performance of the circuit [12]. In Section II, the theory about asynchronous counter is described. Section III describes clock management techniques, Section IV is about simulation result and comparison of delays and Section V is about conclusion. References are described in Section VI.

2.Asynchronous Counters

Asynchronous counter is called as ripple counter. In ripple counter the flip-flop output transition serves as a source for triggering other flip-flops. In other words the clock pulse inputs of all the flip-flops are not triggered by the incoming pulses but rather by the transition that occurs in other flip-flops [2]. The term asynchronous refers to the events that do not occur at the same time. With respect to the counter operation, asynchronous means that the flip-flops within the counter are not made to change states at exactly the same time because the clock pulses are not connected directly to the clock input of each flip-flop in the counter [4].

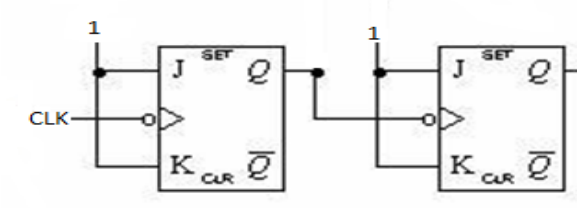

Fig 1 Mod-4 asynchronous counters [2]

Mod-4 counter is 2 bit counter which counts 0 to 3. In this work existing circuit is mod-4 counter which is implemented with clock management techniques.

3.Clock Management Techniques

Pipelining, padding and register insertion are the different techniques implemented in mod-4 asynchronous counter [5]. Pipelining reduces the effective critical path by introducing pipelining latches along the critical data path. The minimum period possible under retiming is restricted by a critical cycle [6]. Critical cycle is maximum average delay cycle i.e. a cycle for which the total delay divided by the maximum no. of registers [11], [13]. In this latches are placed in a path to minimize clock period. In computing a pipeline is a set of data processing elements connected in series, so that the output of one element is the input of the next one. The elements of a pipeline are often executed in parallel or in time sliced fashion [7].

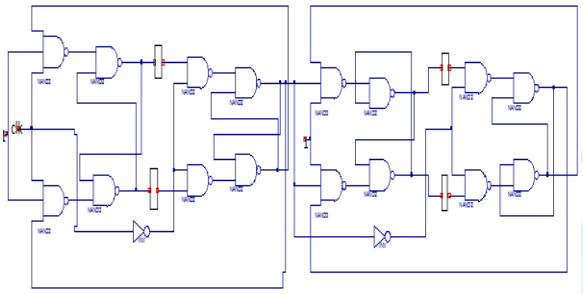

Fig 2 Pipelining in data path

Pipelining transformation leads to a reduction in the critical path i.e. longest path, which can be used it increase the clock speed by using registers along the path [7]. Pipelining transformation leads to a reduction in the critical path or longest path, which can be used to increase the clock speed using registers along the path. This represents different signals will operate independently, new transactions are able to begin while previous transactions are still in progress [14].

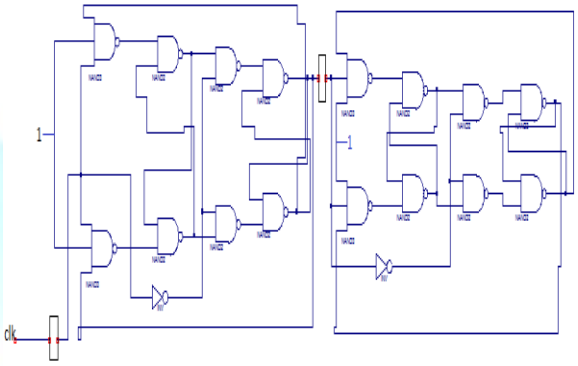

Fig 3 Pipelining in clock path

This represents different signals will operate independently, new transactions are able to begin while previous transactions are still in progress. Padding is nothing but buffer insertion at longest path or critical path. Clock skew scheduling is a useful sequential optimization to improve circuit speed [8].

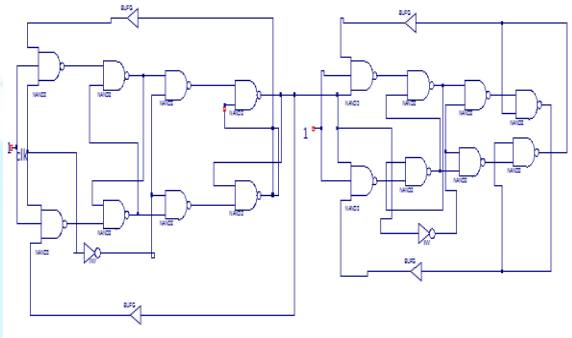

Fig 4 Padding in critical path

By properly scheduling the clock arrival times of registers, the clock period of a nonzero clock skew circuit can be shorter than the longest path delay [9]. However, due to the limitation of hold constraints, clock skew scheduling often cannot achieve the low bound of sequential optimization [8].A hold violation

means the previous data is not held long enough at the destination register. Therefore, the hold violations for achieving the lower bound of sequential timing optimization can be resolved by applying the delay insertion which is referred to as padding method [5].

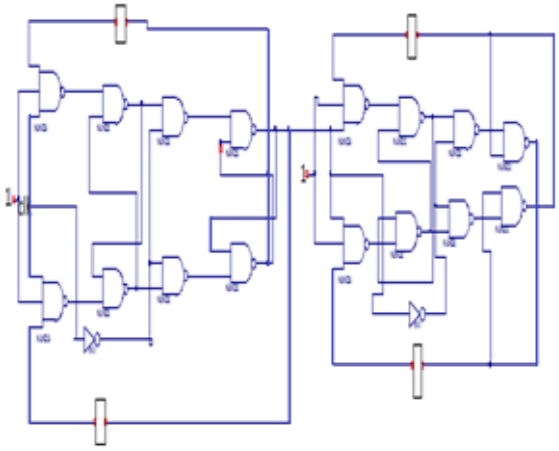

Fig 5 Register insertion in critical path

In longest path which is having more delay after inserting registers and buffers at that path will reduces clock skew [5] and wire delays which are main causes of clock skew and pin delays are reduced. Buffers will amplify the signal when it is placed at the critical paths of the circuit [2].

4.Simulation Results

These graphs represent the simulation result of register insertion at critical path, padding at critical path, pipelining in data path. Simulation has done using Xilinx Software. In Comparison table different delays are discussed.

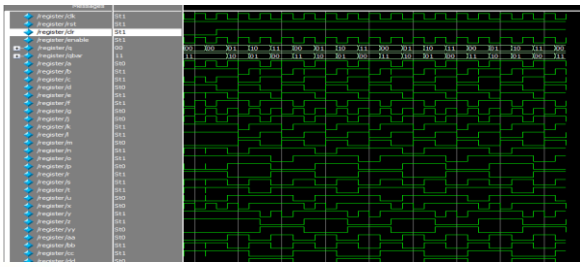

Fig 6 Register insertion at critical path

Fig 6 represents the result about the register insertion at resistive path in the circuit. Registers are inserted at more resistive path in mod-4 asynchronous counter, when clock is negative edge triggered, if reset is '1',clear is '0' and enable is '1' then counter will come to initial state and when clear is '1' circuit starts counting and counts from 0,1,2,3.

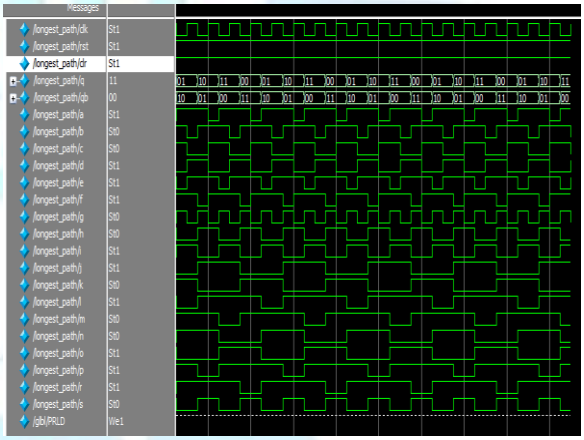

Fig 7 Padding at critical path

Fig 7 describes the output related to padding at resistive path in the circuit. Buffers are inserted at more resistive path in the asynchronous counter, when negative edge triggered clock, if reset is '1', clear is '0' circuit reaches initial state and when clear is '1' circuit starts counting from 0,1,2,3.

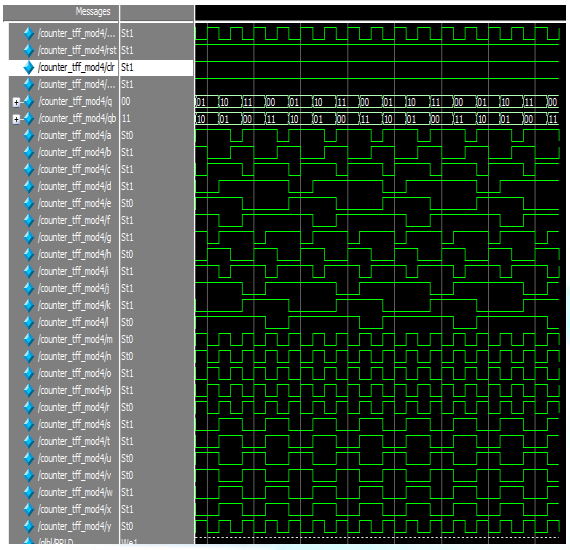

Fig 8 Pipelining in clock path

Fig 8 describes the response of the circuit with pipelining at clock inputs. When reset is '1', enable is '1' and clear is '0' counter will come to initial state and when clear is '1' circuit counts from 0,1,2,3. D-latch has been used for pipelining in clock path of asynchronous counter.

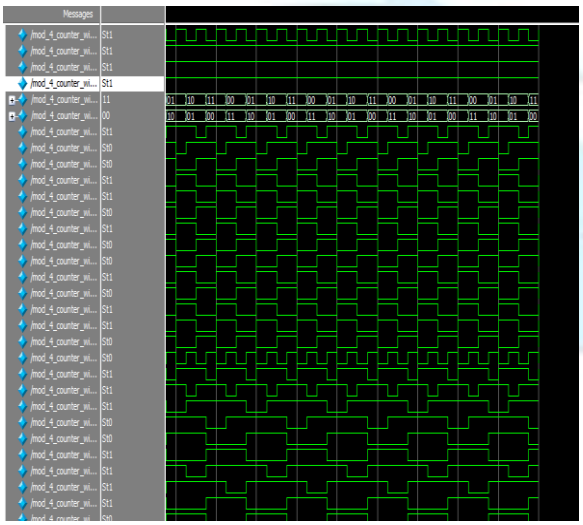

Fig 9 Pipelining in data path

Fig 9 describes the output of the circuit with implementation of pipelining in data path. Pipelining latches are placed in between master and slave section of counter circuit. When clock is negative edge triggered, if reset is '1', at enable '1' and at clear '0' circuit will be at initial state and when clear is '1' circuit starts counting

I. Comparison of Delays:

Parameters	Existing counter	Buffer insertion	Register insertion	Pipelining in clock path	Pipelining in data path
Net Skew (ns)	0.019	0.002	0.001	0.004	0.006
Max delay (ns)	0.741	0.046	1.199	0.046	0.072
Wire delay (ns)	0.895	0.714	0.678	0.606	0.786
Max pin delay (ns)	2.894	2.049	1.615	1.388	2.603
Wire delay on critical nets	1.214	0.959	0.911	1.007	1.426

This table describes comparison of net skew, maximum delay of clock signal of asynchronous counter implemented with different clock management techniques and also describes average connection delay of circuit, maximum pin delay and average connection delay on critical nets in the asynchronous circuit. The net skew was 0.019 ns for existing circuit and 0.004 ns for the circuit implemented pipelining in clock path. The maximum delay of clock was 0.741 ns for existing circuit and 0.046 ns for proposed circuit. The wire delay on critical nets was 1.214 ns for existing and 1.007 ns for the circuit with pipelining at clock input. These

values are from clock report and delay report of the circuits.

5.Conclusion

In this paper, different clock management techniques were implemented in mod-4 asynchronous counter and observed the different delays obtained from timing report. While comparing with existing counter after implementing techniques wire delay, pin delay, connection delay on critical nets and net skew and maximum delay of the clock are minimized. Maximum reduction in delay is obtained by using Pipelining in clock path when compared to other techniques. So, the proposed counter is better in minimizing the clock period compared with existing counter circuit.

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